GaAs MONOLITHIC IMAGE REJECTION DOWN-CONVERTER FOR POINT-TO-MULTIPOINT COMMUNICATION SYSTEMS

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ABSTRACT

A fully integrated GaAs monolithic image rejection down-converter for L/S Band operation is presented. All the necessary subcircuits such as RF splitter, LO phase shifter, two mixers and its biasing circuits are included inside a GaAs chip, and are described. Only an IF hybrid is needed as external component. Experimental results verify the good operation of the device showing more than 20 dB of image rejection, 8 dB gain conversion, 30 dB LO to IF isolation and 20 dB LO to RF isolation throughout the operating band. The MMIC contains 18 MESFETs and 40 passive components in a 1.2 x 3 mm² area.

INTRODUCTION

Image rejection mixers have important applications in microwave systems, especially in broadband communication where a low noise RF amplifier is incorporated in front of the mixer to provide low noise conversion. The rejection of noise bandwidth at the image frequency prevents the degradation of the total system noise figure [1]. For some applications where the IF is sufficiently high and the RF bandwidth narrow enough such that the signal and image frequency bandwidths do not overlap, then the image input can be eliminated by inserting an appropriate band-pass filter in front to a conventional mixer. For broadband applications where the IF frequency is low and the image is therefore too close to the RF and LO frequency it is not practical to filter out the image. The solution is to employ a phasing technique [2,3,4] in order to separate the wanted IF output from the IF image response. This experimented technique, in conjunction with a novel FET mixer configuration [5], has been successfully applied to GaAs technology integration.

The device has been designed for use in a Point-to-multipoint digital radio system. This system is used in the subscriber links of the telephonic network in rural and suburban areas. Each subscriber, or local group of subscribers, have a complete radio system with transmitter and receiver (T/R). As the T/R modules need to be fabricated in a large number, low cost is essential. Because of this, the application is very suitable for monolithic implementation.

PRINCIPLE OF OPERATION

The block diagram of the image rejection mixer consists of two identical mixers, two power dividers and a 90° IF hybrid [fig.1]. The RF signal is fed to the mixers through an in-phase power divider while the LO signal is applied through a quadrature splitter. This introduces a 90° phase difference between the RF and LO signal applied to the mixers, and results in two IF outputs of equal magnitude but in phase quadrature. These outputs are then combined through a 90° IF hybrid. With this arrangement the signals coming from the two RF sidebands appear separated at the two outputs of the hybrid. Separation between signal and image is complete if the gain conversion and phase shifts in the mixers are identical, and the phase and amplitude balances of the hybrids are perfect. However is not possible to obtain a complete symmetry in the mixer circuits and phase and amplitude balances perfection. The image rejection is then limited by overall amplitude and phase imbalance [2] :

$$R_I = -10 \log \left[\frac{1 - 2\sqrt{G}\cos(\theta) + G}{1 + 2\sqrt{G}\cos(\theta) + G} \right]$$

where θ is the phase imbalance and G is the gain imbalance. Achieving 20 dB image rejection requires that the phase error be kept below 10° and the gain imbalance below 1 dB. Symmetry achieved by monolithic implementation of mixers and lumped elements hybrids on a single chip assures very good and practical image rejection also in mixers with wide RF bandwidth and low IF frequency.

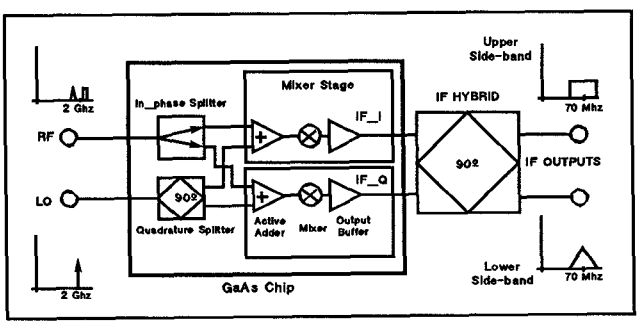

Fig. 1. Block Diagram of the Image-Rejection Down-Converter.

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CIRCUIT DESIGN

Quadrature and In-phase Splitters

The local oscillator is split in two components of the same amplitude and delayed by 90° by using a passive network. It is composed of two sections low-pass/high-pass (fig.2b) designed to shift +45°/-45°. This network allows one-octave bandwidth (1.5-3 GHz) and has been optimized not to be sensitive to the fabrication process, especially to the capacitor tolerance [6].

A Wilkinson divider (fig.2a) is used to split the RF signal in two in-phase components, keeping an appropriate input impedance. Each one of these is separately multiplied by one of the oscillator components in a mixer cell.

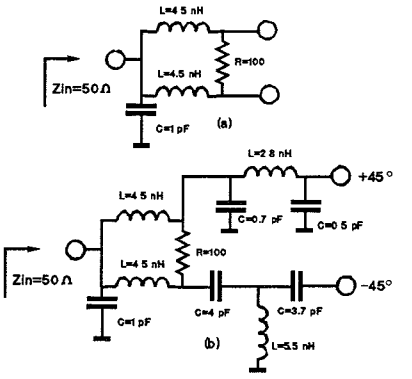

Fig. 2. In-Phase Splitter (a) and Quadrature Splitter (b).

Active Adder

The first section of each mixer cell is the active adder (fig.3), which combines the RF and LO signals. It consists of two common-gate FETs. Each of these FETs presents at its source an input impedance equal to $1/g_m$, where g_m is the transconductance of the FET. Choosing the FET gate width so g_m=20mS, this impedance will be 50 Ω. This is important not only to get a good input matching, but to load the filters of the quadrature splitter with a known and precise impedance.

The active adder isolates the RF and the LO ports because of the unilateral behaviour of the transistors.

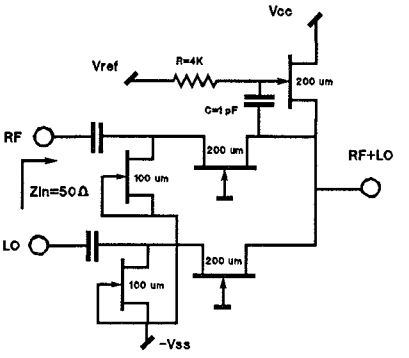

Fig. 3. Active Adder.

Mixer Stage

The mixer element is a 0.8 x 600 μm Single-Gate FET (fig.4a), which is driven at its gate by the sum of the LO and RF. Because of the non linearity of its transconductance, the sum and difference signals of frequencies between LO/RF appear at its drain.

To get the maximum conversion efficiency, the FET should be biased at the point where the derivative of the transconductance is maximum. This point is close to the pinch-off of the FET.

A filter consisting of a capacitor eliminates the sum of frequencies signal, the LO and the RF, so only the frequency difference signal -the IF- remains.

An input matching network composed of two inductors, is placed at the gate of the mixer FET to match its impedance with the active adder output, and to equalize the conversion gain. This network also grounds any spurious signals or noise at the IF frequency that could be present at the FET gate. Otherwise it would be amplified by the mixer FET and would appear at the output.

Due to the large frequency difference between LO/RF (about 2 GHz) and IF (less than 100 MHz) it is not necessary to use a balanced configuration to separate them.

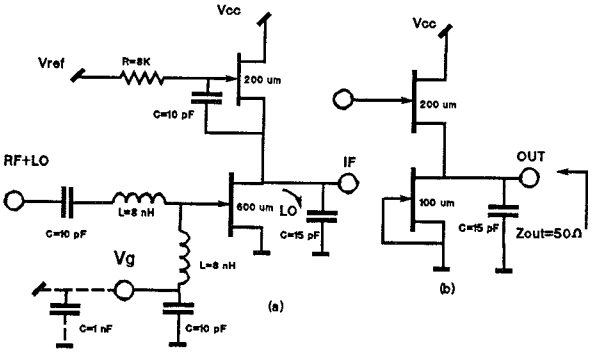

Fig. 4. Mixer Stage (a) and Output Buffer (b).

Output Stage

A source-follower output stage (fig.3b) is used to amplify the IF signal. The FET size has been chosen to guarantee an output impedance of 50 Ω at IF frequency. This is important to drive the external IF hybrid with a precise and known impedance. A capacitor is used to achieve supplementary suppression of LO/RF.

This stage is DC-coupled to the mixer drain, so any value of the Intermediate Frequency from DC to 100 MHz can be used.

Biasing

In order to achieve a small chip area, a full active bias is used in all the circuit. The current is injected to the source of common-gate and common-drain FET by FETs working as current sources. Active loads are used in all the stages. To avoid the stability problems at DC of the conventional active loads, frequency dependent active loads have been used (fig. 3,4) [7]. At high frequency, the capacitor between gate and source of the load behaves as a short circuit, so the FET presents R_{ds} as source impedance. At DC, the FET behaves as a source-follower stage and the impedance shown at the source is $1/g_m$, much lower than R_{ds}.

In a non-linear circuit, the value of the DC-current that flows by a FET changes not only by the bias voltage supplied to its gate but also by the RF power level. If a conventional active load were used, any change in the DC-current would produce a large variation on the voltage at the drain of the active FET.

Modelling and Simulation

The circuit has been designed using LIBRA harmonic balance program [8]. A non-linear model for the MESFET was especially developed for this design, based on Curtice cuadratic model [9]. The parameters of the model were calculated using an in-house software. Experimental results well matched simulations, demonstrating the validity of the model. The linear mode of LIBRA (TOUCHSTONE) was used to refine the simulation of the linear subcircuits.

LAYOUT AND FABRICATION

In order to fulfil the low-cost requirement of the project, a MESFET fabrication process with a gate length of 0.8 μm has been selected and a design without via-holes were chosen to achieve a high fabrication yield.

The use of FETs instead of inductors for biasing allows a high-density layout (1.2 x 3 mm^2). Fig. 5 shows a photograph of the device.

Special attention has been paid to the symmetry between the two mixer sections. The use of a technology without via-holes forces to a rectangular shape to get short the ground connections.

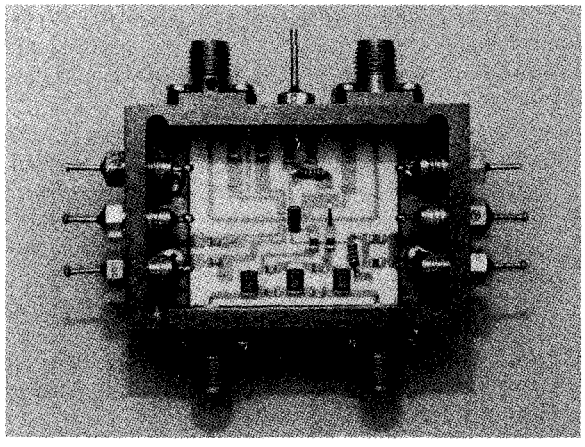

Fig. 6. Photograph of the circuit test fixture.

EXPERIMENTAL RESULTS

The circuit was mounted on a testing jig (fig. 6) and tested in the whole RF bandwidth (1.5 -3 GHz) at different IF frequencies (from 30 to 100 MHz). The necessary local oscillator power for maximum efficiency is between -5 and 0 dBm. The input matching at the LO and RF ports is betterthan -15 dB over the full bandwidth. The output impedance at the IF ports is also close to 50 Ω.

The RF to LO isolation is of about 20 dB all over the band, demonstrating the good operation of the active adder (Fig 7).

Fig 8 shows the conversion gain and noise figure versus RF frequency for a fixed IF of 70 MHz. The conversion gain slows down with the IF frequency due to the RF filter capacitors, as we can see in fig 11 showing the signal and image responses versus IF for a fixed LO of 2 GHz. In this figure also the image rejection can be appreciated. For this measurement, a commercial stripline coupler, centred at 75 MHz, was used as IF hybrid. At this frequency the image rejection, defined as difference between signal and image response is as good as 40 dB. At different frequencies the IF hybrid introduces an error that decreases the image rejection.

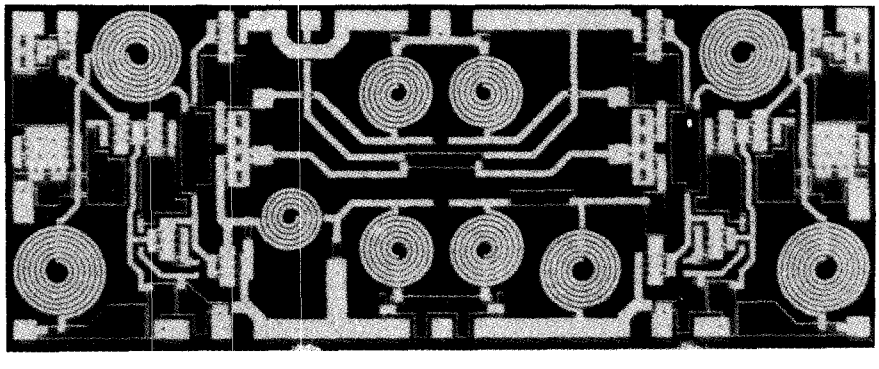

Fig. 5. Photograph of the chip.

Similar results were obtained using an IF of 30 MHz and a lumped-type hybrid. If the phase and amplitude balances of the hybrid are perfect, the image rejection is about 40 dB.

These results show that the image rejection is limited by the performance of the IF hybrid, while the operation of the GaAs MMIC is very good. This can be also demonstrated by observing the two IF outputs of the MMIC, IF_I and IF_Q (fig. 10) in an oscilloscope. The delay between them is 90° with an error of less than ± 7° over the full bandwidth.

For practical receivers using IF hybrids made with standard low-cost components, and without any tune or adjustment, the image rejection is about 20 dB. This value can be easily improved to 30 dB if the IF hybrid is made with precision or adjustable components.

CONCLUSION

A full-integrated Image-Rejection down-converter designed for low-cost mass production has been presented and the circuits that made it up have been described. All the necessary RF circuits as phase shifter, divider, mixers, output stages and bias are included inside a 1.2 x 3 mm^2 GaAs chip. The experimental results demonstrate a gain of about 10 dB and more than 30 dB of image suppression in the 1.5-3 GHz RF band.

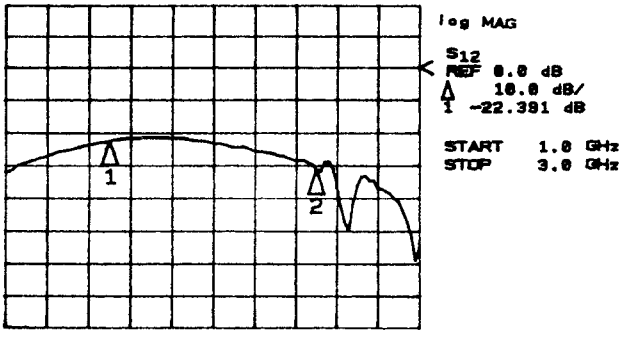

Fig. 7. LO to RF isolation.

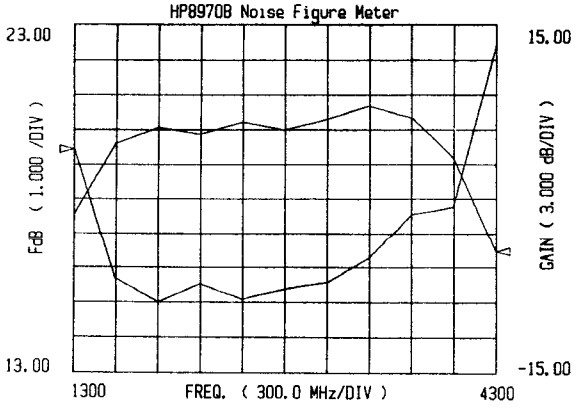

Fig. 8. Conversion Gain and Noise Figure sweeping RF and LO for a fixed IF of 70 MHz.

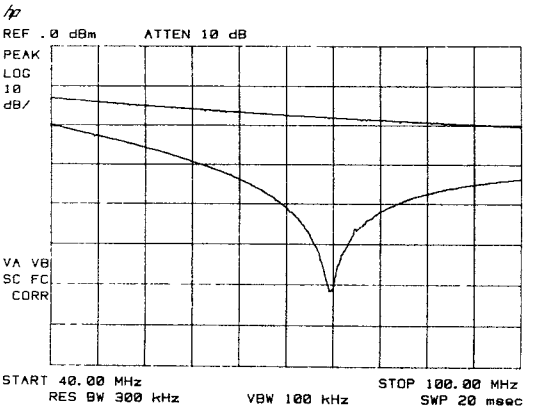

Fig. 9. RF sweep (LO fixed at 2 GHz) in a spectrum analyzer showing signal and image response versus Intermediate Frequency.

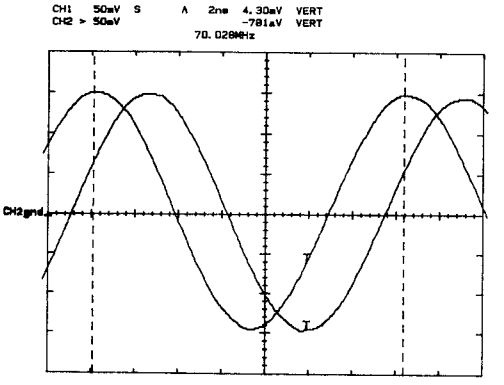

Fig. 10. Oscilloscope traces of the signals IF_I and IF_Q (outputs of the GaAs chip) before the IF hybrid.

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